

FIG.1

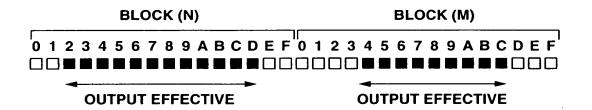


FIG.2

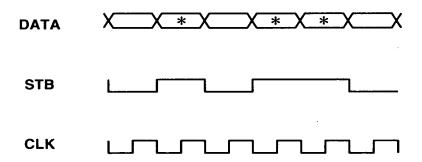


FIG.3

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FIG.4A PB_DATA	¥	2X	XE	4X	50\jump>		
FIG.4B BUFF_WR		5X	3×	**			
FIG.4C Ecc			X	XX	X4		
FIG.4D NAVI_DET			2X	XE	4X		
			INEW_E	INEW_ESA_SET			
FIG.4E BUFF_RD				5	3X	4X	
FIG.4F VIDEO_DEC					l_pic(new)		
FIG.4G DISPLAY					l_pic(old)		l_pic(new)

FIG.5A PB_DATA 1X ⟨jump⟩ **2X 3X** FIG.5B BUFF_WR ⟨WR_STOP⟩ **2X 3X** FIG.5C ECC (ECC_STOP) **2X** FIG.5D NAVI_DET **2X** INEW_ESA_SET $\langle \mathtt{RD_START} \rangle$ $\langle RD_STOP \rangle$ FIG.5E BUFF_RD 2X FIG.5F VIDEO_DEC FIG.5G DISPLAY l_pic(old)

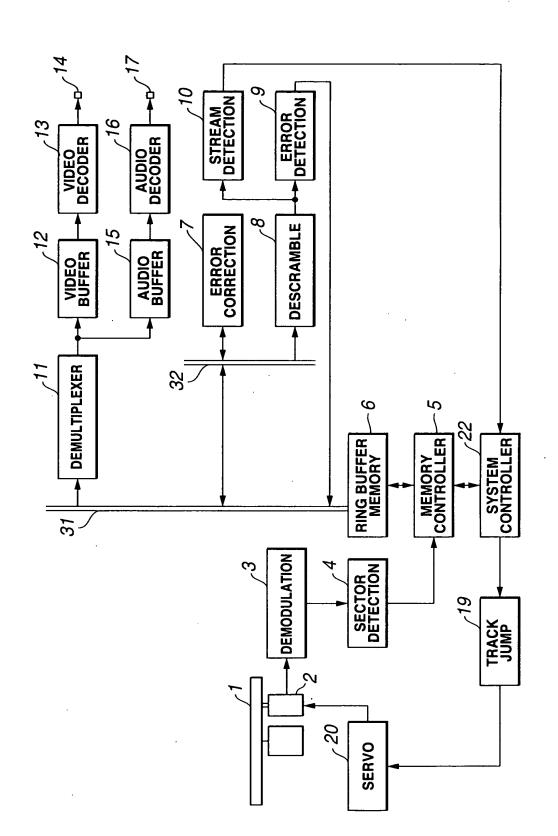


FIG.6

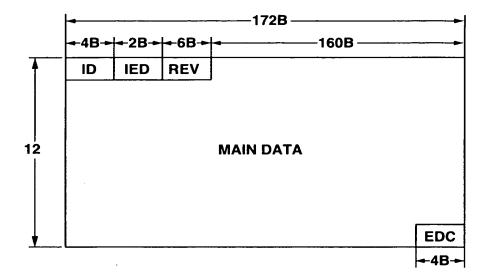


FIG.7

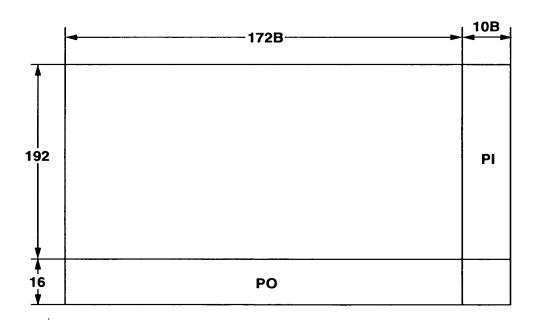


FIG.8

32BITS	1456BITS	32BITS	1458BITS
SY0	ID IED	SY5	P1
SY1		SY5	P1
SY2		SY5	P1
SY3		SY5	P1
SY4		SY5	P1
SY1		SY6	P1
SY2		SY6	P1
SY3		SY6	P1
SY4		SY6	P1
SY1		SY7	P1
SY2		SY7	P1
SY3		SY7	EDC P1
SY4	P0	SY7	P0 P1

FIG.9

FIG.10A

NV_PCK#n
PCI DSI

FIG.10B

PSI_GI NSML_AGL I HL I REC I

FIG.10C

	Content
(1)NV_PCK_LBN	LBN of Navigation pack
(2)VOBU_CAT	Category of VOBU
reserved	reserved
(3)VOBU_UOP_CTL	User Operation control of VOBU
(4)VOBU_S_PTM	Start PTM of VOBU
(5)VOBU_E_PTM	End PTM of VOBU
(6)VOBU_SE_E_PTM	Eun PTM of scqurnce end in VOBU
(7)C_SLIM	Cell Elpse Time

FIG.11A

NV_PCK#n
PCI DSI

FIG.11B

DSI_GI SML_PBI SML_AGL I VOBU_SRI SYNC I

FIG.11C

	Content
(1)NV_PCK_SCR	SCR_base of NV_PCK
(2)NV_PCK_LBN	LBN of NV_PCK
(3)VOBU_EA	End address of VOBU
(4)VOBU_1STREF_EA	End address of the first Reference Picture in VOBU
(5)VOBU_2NDREF_EA	End address of the second Reference Picture in VOBU
(6)VOBU_3RDREF_EA	End address of the third Reference Picture in VOBU
(7)VOBU_VOB_I DN	VOBU ID number of the VOBU
reserved	reserved
(8)VOBU_C_I DN	Cell ID number of the VOBU
(9)C_ELTIM	Cell Elpse Time

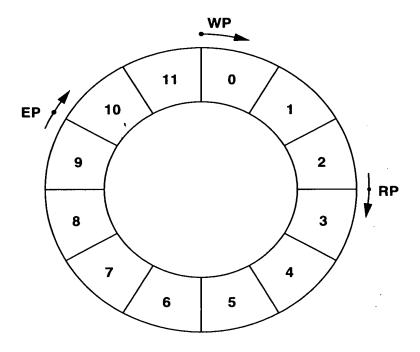


FIG.12

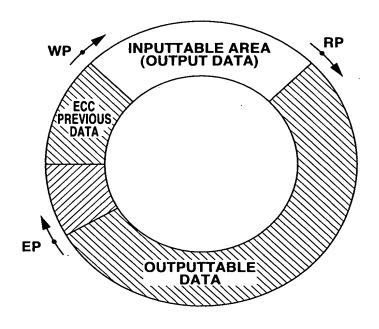


FIG.13

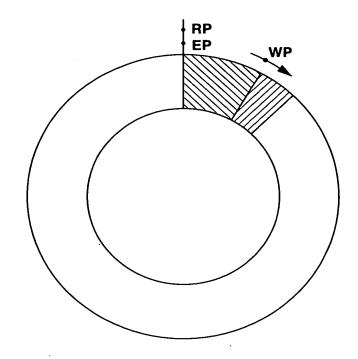


FIG.14

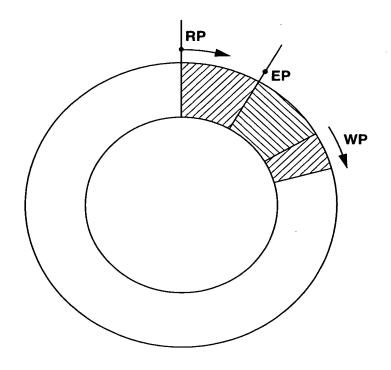


FIG.15

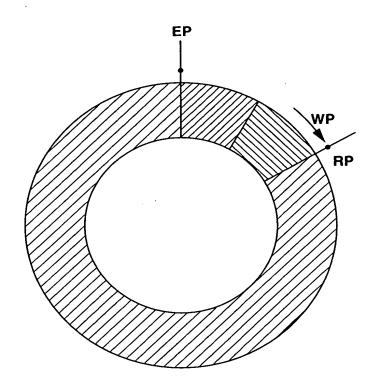


FIG.16

		BLOCK (N) BLOCK (N+1)
FIG.17A BUFF_WR	BUFF_WR	0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 8 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 8 8 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 8 8 8 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
FIG.17B	START SECTOR	001000000000000000000000000000000000000
FIG.17C	END SECTOR	000000000000000000000000000000000000000
FIG.17D	OUTPUT SPECIFYING SECTOR	00111111111111111111000000000
FIG. 17E	NAVI SECTOR	001000000000000000000000000000000000000
	CORRECTION RESULT FLAG	000000000000000000000000000000000000000
FIG.17G	IP OUTPUT SECTOR	00111111111111111111100000000
FIG 17H BUFF	BUFF RD	

	BLOCK (N) BLOCK (N+1)
FIG.18A BUFF_WR	0123456789ABCDEF0123456789ABCDEF
FIG.18B START SECTOR	001000000000000000000000000000000000000
FIG.18C END SECTOR	000000000000000000000000000000000000000
FIG.18D OUTPUT SPECIFYING SECTOR	001111111111111111111111111111111111
FIG.18E NAVI SECTOR	001000000000000000000000000000000000000
FIG.18F CORRECTION RESULT FLAG	000000000000000000000000000000000000000
FIG. 18G POUTPUT SECTOR	001000000000000000000000000000000000000
FIG. 18H BUFF_RD	000000000000000000000000000000000000000

FIG.19A PB_DATA (jump) 1X **2X 3X** FIG.19B BUFF_WR ⟨WR_STOP⟩ **2X 3X** FIG.19C ECC **2X** ⟨ECC_STOP⟩ NAVI_DET INEW_ESA_SET IP_END_DET IIP_END_DET FIG.19E BUFF_RD 2X FIG.19F VIDEO_DEC FIG.19G DISPLAY l_pic(old)